Angular Dependence of Multiple-Bit Upsets Induced by Protons in a 16 Mbit DRAM

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***Abstract*—The number of double-bit upsets induced by protons in a 16 Mb DRAM was found to increase with angle of incidence. The increase was greater for intermediate energy (63 MeV) protons than for high-energy (198 MeV) protons. An explanation is offered and the results of a calculation using the CUPID program agree with the observations.**

***Index Terms*—CUPID, DRAM, linear energy transfer (LET), single event upset (SEU).**

I. Introduction

SINGLE EVENT UPSET (SEU) cross sections for electronic circuits vary with angle of incidence for both heavy-ion and proton irradiation. However, the underlying mechanisms are different: For heavy ions, angular effects are related to the increase with angle of the ion's path-length through the sensitive volume, whereas for protons, they are caused by anisotropic inelastic nuclear scattering. Varying angle of incidence to increase effective linear energy transfer (LET) is routinely done when measuring SEU cross sections with heavy ions, but is generally ignored for protons because the effects on SEU cross section have, for the most part, been small [1], [2].

Predictions were recently confirmed that significant angular effects would be observable in the proton-induced SEU cross sections for thin devices with large aspect ratios, typical of modern devices [3]–[5]. One such confirmation reported an order of magnitude increase in the SEU cross section for 63 MeV protons incident at grazing angle on an SOI device with a thin (0.5 μm) silicon layer. These results suggest that future measurements will have to include large angle measurements, particularly for thin epitaxial and SOI devices.

In this paper, we report the first observation of an increase in the cross section for double-bit upsets induced by protons at large angles of incidence. Measurements were made on a 16 Mbit DRAM processed in bulk silicon for which the device geometry differs significantly from that of the SOI devices previously tested. The data revealed an enhancement in the double-bit upset cross section for large angles of incidence. The enhancement was greater for 63 MeV protons than for 198 MeV protons. The increase in the double-bit upset cross section at grazing incidence was not accompanied by a concomitant increase in the cross section for single bits.

Proton-induced MBUs were modeled using the CUPID program together with information about the device structure [5]. The results of the calculations explain qualitatively how the increase in the number of double-bit upsets at grazing angle is related to anisotropic inelastic scattering. They also suggest that, as devices become more densely packed, angular effects will become increasingly more evident in measurements of multiple-bit upset cross sections.

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II. Background

A. First-Order SEU Model

Heavy ions produce SEUs by liberating charge in or near sensitive nodes. An upset occurs when the amount of collected charge $(Q_{\rm col})$, which is some fraction of the charge liberated by the heavy ion, exceeds the device's critical charge $(Q_{\rm crit})$. Neglecting funneling and diffusion, the collected charge is proportional to the product of the ion LET and the path length through the sensitive volume. At normal incidence, the path length is just the thickness (d) of the sensitive volume, and $Q_{\rm col}$ is the product of LET and d. By increasing the angle of incidence of the incoming ion, the path length and, consequently, the amount of charge deposited in the sensitive volume is increased by a factor sec (θ), where θ is the angle of incidence. Below saturation, the SEU cross section increases with LET and, therefore, with angle. Even though there are clear weaknesses to this first-order model, it is routinely used for heavy-ion SEU rate predictions.

The situation for protons is quite different. In most cases direct ionization from protons is insufficient to produce upsets in electronic components, even at grazing incidence. However, approximately 1 in 10^5 incident protons will collide with a nucleus and some of the particles emerging from the collision will have sufficient LETs and ranges to produce SEUs. As long as the device is smaller than the proton beam, the scattering cross section is independent of angle of incidence. Angular effects arise as a result of the scattering process itself, which consists of both elastic and inelastic components, both of which depend on proton energy. At the energies involved in this work, elastic scattering is small and may be ignored. That leaves inelastic scattering, which has been shown to be anisotropic, with a greater number of particles scattered in the forward direction to conserve momentum.

The energy-dependence of the anisotropic emission of spallation products has been explained using the cascade-evaporation model, which describes inelastic scattering as consisting of two steps [6]. The cascade stage involves the collision between the proton and individual nucleons, some of which are ejected from the nucleus. The evaporation stage involves the de-excitation of the nucleus through the emission of nuclei with atomic masses spanning the range up to silicon. During the cascade stage the nucleons emerge from the nucleus isotropically. The angular distribution of the inelastically scattered nuclei depends on the incident proton energy, being more forward directed at higher energies to conserve momentum [5]. However, at higher proton energies (198 MeV) the nuclei emitted at 90° also have higher energies and, therefore, being on the rising side of the Bragg peak, higher LETs than is the case for the lower energy (63 MeV) protons.

Enhancement of the proton SEU cross section at grazing angle depends on a number of factors, including device geometry, proton energy and critical charge. Device geometries most susceptible to angular effects are those with one dimension (usually thickness) much smaller than the other two. Spallation products are emitted with a spread in energy, LET and range and those with the highest LETs and longest range are emitted preferentially in the forward direction. At normal incidence the sensitive volume is too thin even for high-LET ions to produce SEUs, but at grazing incidence the path lengths of the forward scattered ions through the sensitive volume are greatly increased, making it more likely they will deposit sufficient charge to produce SEUs.

Proton energy and $Q_{\rm crit}$ are the other two factors determining whether enhanced SEUs cross sections will be observed at grazing angles of incidence. There is a subtle interplay between these two parameters for the effects to be observed. As already pointed out, the angular distribution of scattered ions is more forward directed at higher energies. Those ions emitted perpendicular to the direction of the incident protons will also have higher energies and, therefore, higher LETs. For intermediate values of $Q_{\rm crit}$ ($\rm LET_{th} \sim 10$ MeV·cm^2/mg), the laterally emitted ions from 200-MeV proton inelastic scattering should be able to produce SEUs. Consequently, there can be no SEU enhancement at large angles of incidence. However, the laterally scattered ions from 63-MeV protons should not have sufficient energy to produce SEUs. Then, when the protons are incident at large angles, there can be enhancement in the SEU cross section because the forward-scattered ions will have sufficient energy (LET) and range for their product to exceed $Q_{\rm crit}$. Evidently, there can be no SEU enhancement for values of $Q_{\rm crit}$ that are either very small or very large. They are best observed for intermediate values.

The above explanation was invoked to explain the recent observation in SOI devices of an order of magnitude increase in the SEU cross section for 63 MeV protons and no enhancement for 200 MeV protons [5].

B. Previous Measurements

The possibility of an enhanced SEU cross section for devices exposed to protons incident at grazing angle is a concern because ignoring angular effects could lead to significant errors in calculations of SEU rates in space. Over the years there have been sporadic reports concerning the presence or absence of effects of proton angle-of-incidence on SEU cross section. Initial measurements by Nichols *et al.* failed to find any angular effects in a variety of different devices exposed to 590 MeV protons [1]. Subsequent measurements by Koga *et al.* revealed a modest (factor of two) increase in SEU cross section between 0° and 60° for four different types of SRAMs exposed to 50 MeV protons [7]. Shortly thereafter, measurements were carried out by Levinson *et al.* on 16 Kbit CMOS SRAMs and thin surface barrier detectors exposed to protons over an energy range from 50 to 300 MeV [2]. Only a weak anisotropy was measured, in agreement with their theory. Next, Reed *et al.* predicted that SEUs in circuits with high LET thresholds and relatively thin sensitive volumes would likely exhibit significant angular effects with proton irradiation [3], [4]. However, Reed *et al.* failed to observe an increase in the multiple-bit upset cross section in a 256 Kbit SRAM, due to the large separation between the memory cells [8]. At about the same time, Gardic *et al.* observed increases in the SEU cross section for a 256 Kbit SRAM exposed to 100 MeV and 200 MeV protons at grazing angles [9]. Predictions that SOS and SOI structures were ideally suited for observing angular effects were confirmed experimentally by Reed *et al.* [5].

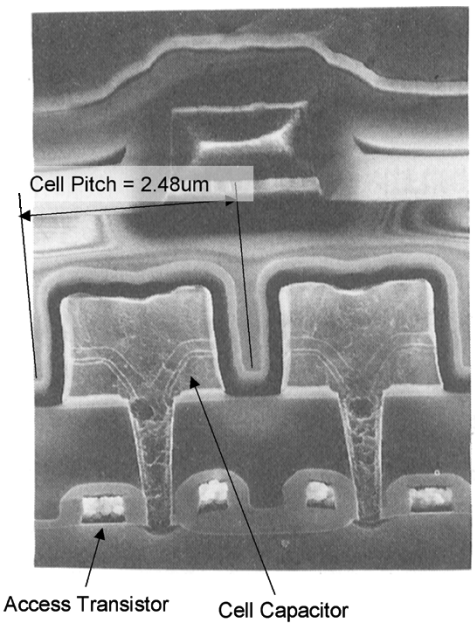

Fig. 1. Cross-sectional electron micrograph of two adjacent DRAM storage cells parallel to the "word lines."

In modern memory devices angular effects should be observable in both SEUs and MBUs, provided the right combination of geometry, device critical charge and proton energy prevail.

Previous publications have documented the proton and heavy ion upset measurements [10]–[12] and have presented results of a space experiment (the Microelectronics and Photonic Testbed, MPTB), which included these same parts, along with some SEU and MBU modeling.

III. Device Description

The devices tested were 16 Mbit DRAMs manufactured in bulk p-type silicon substrates by NEC. Each memory cell consisted of an n-channel access transistor and a capacitor located over the bit line. Fig. 1 shows an electron-microscope image of

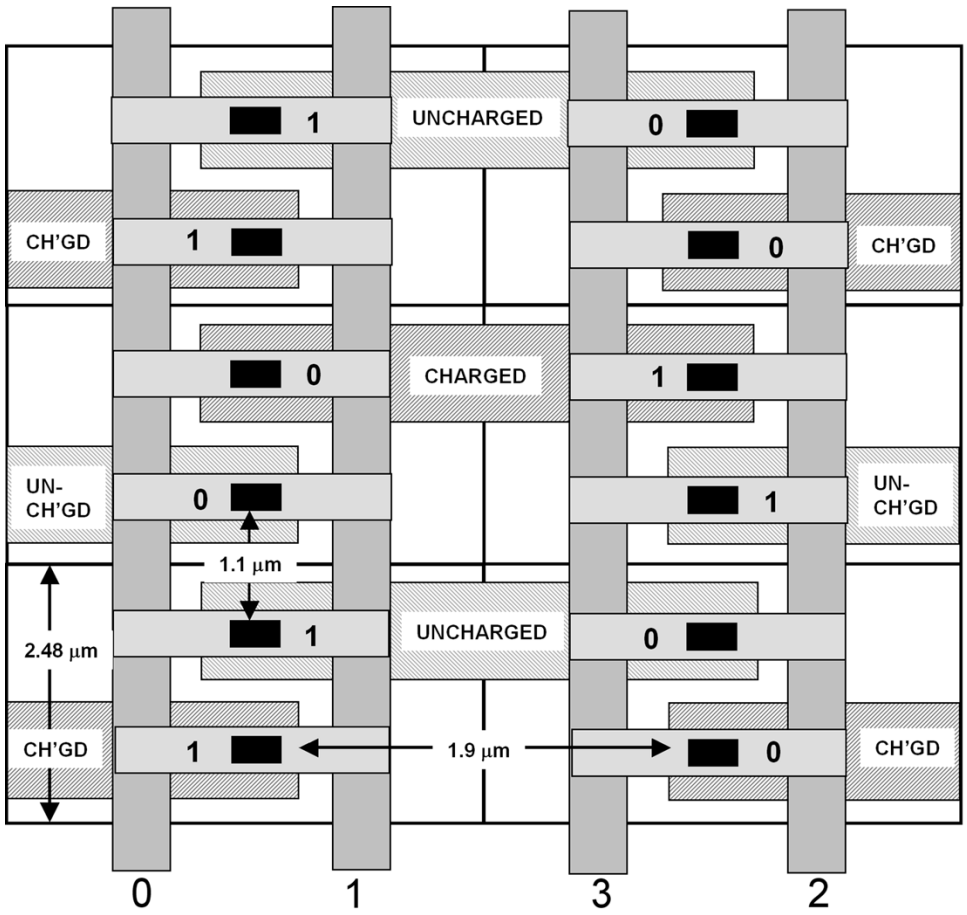

Fig. 2. Layout of the 16 Mbit DRAM showing the state of the cells when a checkerboard pattern is written to the DRAM. The "word" lines are marked "0," "1," "2," and "3."

the cell's cross section. The capacitor has a relatively large capacitance of 27 fF. SEUs occur when an ion deposits charge in the drain of the access transistor that is sufficient to discharge the capacitor. With the access transistor located in bulk Si, charge may be collected via both drift and diffusion. Heavy-ion measurements indicate that the part is very sensitive to SEUs, having a LET threshold of about 0.6 MeV·cm^2/mg.

For testing a checkerboard pattern of "1 s" and "0 s" was written to the DRAM. SEUs occur only when capacitors are discharged. To maintain balance, half the cells are charged when they store a "1" and the other half are charged when they store a "0." This was confirmed by the upset data that showed that upsets occurred for both $1- > 0$ and $0- > 1$ transitions. Fig. 2 shows the layout of the cells and indicates which ones are charged and which ones are uncharged when the DRAM contains a checkerboard pattern of "1 s" and "0 s." The pitch parallel to the bit lines is 2.48 μm and parallel to the word lines is 1.1 μm. The short distance (1.1 μm) between the centers of the charged cells along the direction of the word lines are those most likely to be involved in MBUs. The next closest distance between sensitive cells is between two charged cells along the bit line (1.9 μm).

IV. Experiment

SEU testing was carried out at two facilities—Crocker Nuclear Laboratory, University of California at Davis with 63-MeV protons and Indiana University Cyclotron Facility with 198-MeV protons. Testing was done as a function of angle of incidence by rotating the device around two perpendicular axes, one parallel to the word lines and one parallel to the bit lines. More than a thousand events were recorded, but only about 40 double-bit upsets were recorded at normal incidence. The parts were encapsulated in plastic so normally incident protons had to pass through 0.42 mm of plastic before reaching the silicon. With increasing angle, the effective thickness of the plastic increased as well. It was possible to identify MBUs in the DRAM because we had the bit map relating logical to physical addresses.

V. Results

Fig. 3 shows the number of double-bit upsets as a function of proton angle of incidence for 63 MeV protons for the case where the device was rotated around an axis parallel to the "bit" lines of the DRAM. The fluence was the same for all the runs, so the cross section for double bit upsets is obtained by dividing the number of double-bit upsets by the fluence (2.26×10^9/cm^2).

There is a gradual increase in the number of double-bit upsets with increasing angle such that near 90° the number has increased by a factor of three.

Fig. 4 shows the number of double-bit upsets as a function of proton angle of incidence for the case where the part was rotated about an axis parallel to the "word" lines of the DRAM

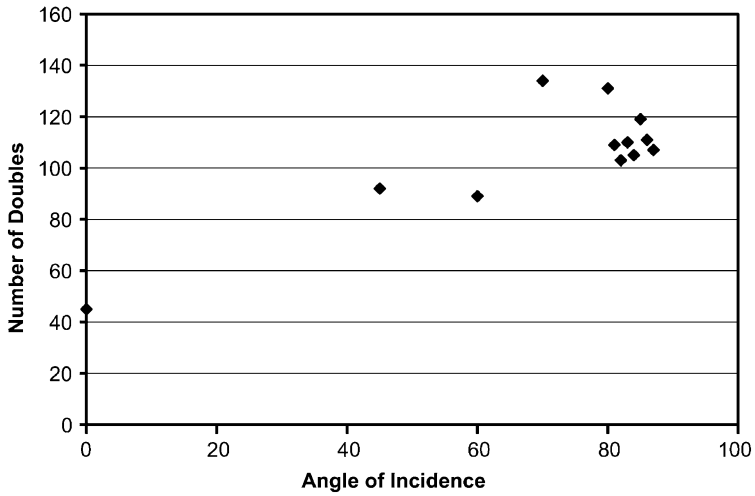

Fig. 3. Number of double-bit upsets as a function of proton angle of incidence for a fixed fluence of 63 MeV protons incident on the NEC DRAM. The axis of rotation was parallel to the "bit" lines.

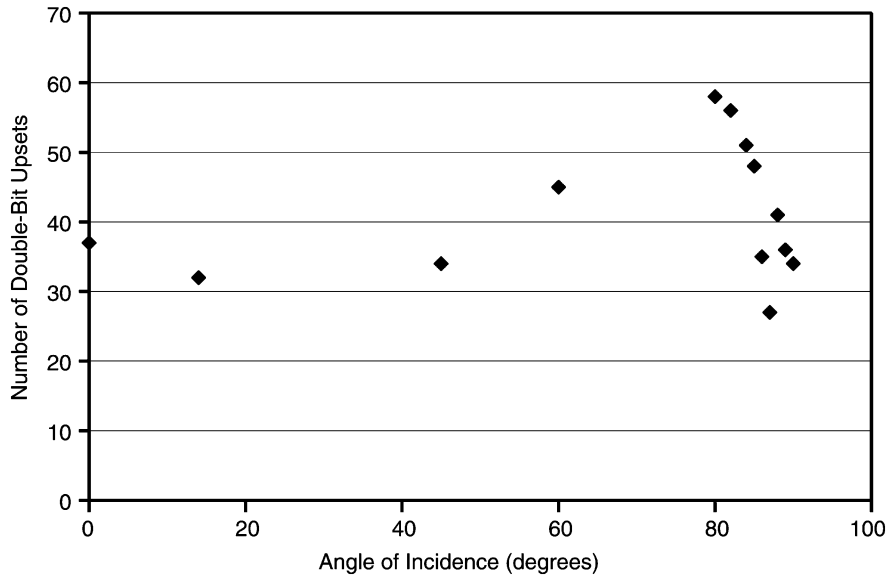

Fig. 4. Number of double-bit upsets as a function of proton angle of incidence for a fixed fluence of 63 MeV protons incident on the NEC DRAM. The axis of rotation was parallel to the "word" lines.

cells. All data points were for a fixed fluence ($1.5 \times 10^9/\text{cm}^2$), which was $2/3$ of the fluence used for the data in Fig. 3. The data show a much smaller enhancement with angle of incidence. In both cases the number of double-bit upsets drops off near 90°. In both cases the drop-offs are not due to shadowing or mechanical effects.

Fig. 5 shows the total number of events (SEUs and double-bit upsets) as a function of angle of incidence for 63-MeV proton irradiation. The angle of rotation is parallel to the "bit" lines. There is a decrease in the total number of events of about 25%.

Fig. 6 shows the number of double-bit upsets as a function of angle of incidence for 198 MeV protons. The data exhibit an enhancement of approximately two near grazing incidence. The double-bit upset enhancement is smaller for 198 MeV protons than for 63 MeV protons. At normal incidence, the data for 198 MeV protons contain more total events and more double-bit upsets. Fig. 7 shows that the number of events does not change with angle of incidence for the 198 MeV protons.

VI. Discussion

The results presented in the previous section describe the effects of angle of incidence on the number of single-bit and double-bit upsets induced in a 16 Mbit DRAM by energetic protons incident over a range of angles. No enhancement with angle of incidence was observed for single-bit upsets, a result that was expected because of the access transistor's small critical charge and large (due to diffusion) isotropic collection volume in bulk silicon. In contrast, there was a pronounced increase in the number of double-bit upsets observed at large angles of incidence. The enhancement was greater for 63 MeV protons than for 198 MeV protons.

Upsets in DRAM cells are caused by the discharge of capacitors, never the reverse. Free carriers generated at or near the drain of the n-channel access transistor are collected across the drain/substrate junction, thereby discharging the capacitor. To maintain electrical balance, charged cells are designed to represent either a "1" or a "0." An upset may then be associated with

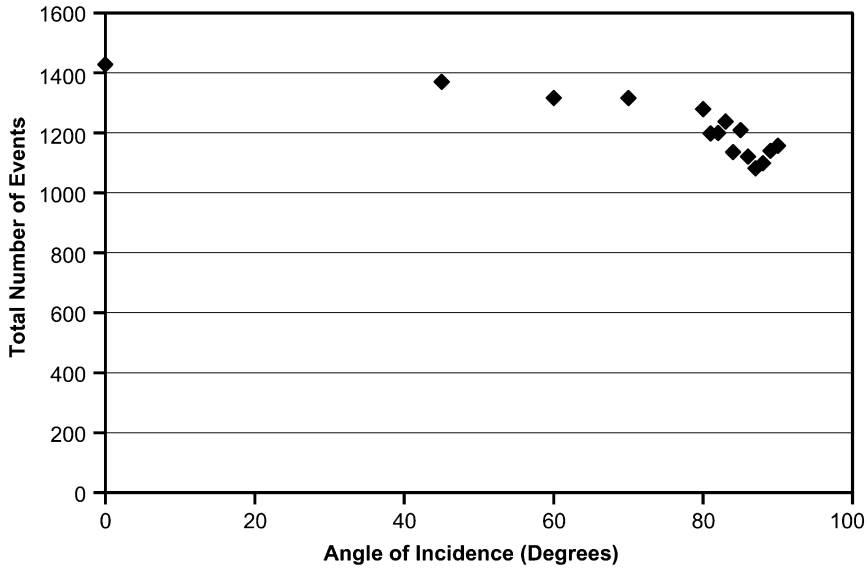

Fig. 5. Total number of events (single-bit and double-bit) as a function of proton angle of incidence for a fixed fluence of 63 MeV protons incident on the DRAM. The angle of rotation was parallel to the "bit" lines.

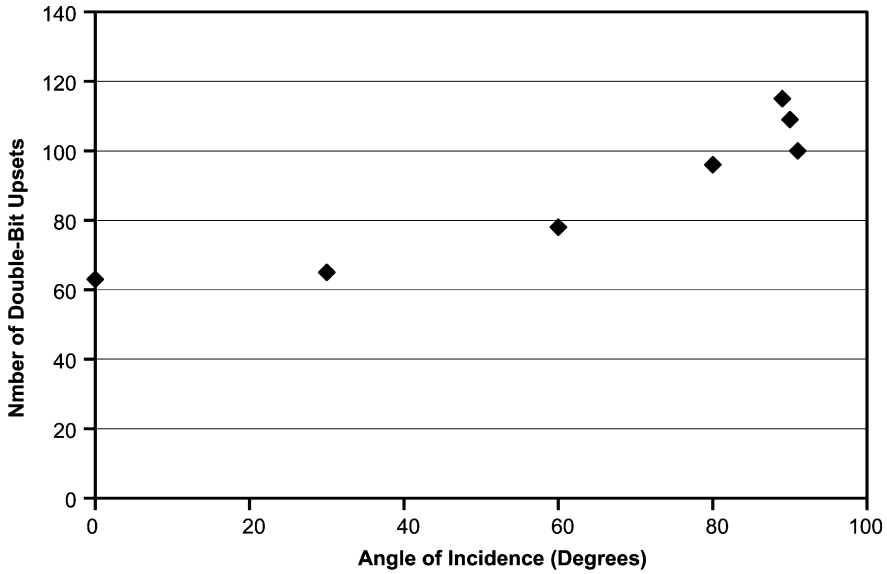

Fig. 6. Number of double-bit upsets as a function of proton angle of incidence for a fixed fluence of 198 MeV protons incident on the NEC DRAM. The angle of rotation was parallel to the "bit" lines.

either a "1" switching to a "0" or vice-versa. In the experiments reported here, the cells were always filled with a checkerboard pattern of "1 s" and "0 s," and every double-bit upset consisted of one cell going from a "1" to a "0" and the other going from a "0" to a "1." Fig. 2 shows the charge states of the cells as well as the digital data stored in them. The figure clearly shows that the second and third cells from the top in both columns can contribute to double-bit upsets when the path of a spallation ion passes through or near the drains of the two adjacent access transistors.

Fig. 3 shows that at normal incidence there are approximately 40 double-bit upsets. The number is energy-dependent, dropping to zero at 20 MeV and increasing to around 60 at 198 MeV.

The data in Fig. 3 were taken by rotating the device around an axis parallel to the bit lines, which run horizontally in Fig. 2. Double-bit upsets are due to the simultaneous discharge of the two closest charged cells. For example, the second and third cells from the top in the first column are charged, and both can participate in double bit upsets. By rotating the DRAM around an axis parallel to the bit lines, the protons' angle of incidence is increased, and so is the number of double-bit upsets.

Fig. 4 is a plot of the number of double-bit upsets as a function of proton angle of incidence when the axis of rotation is parallel to the word line. The number of double-bit upsets is seen to increase with angle of incidence, but the increase is much smaller than for rotations around an axis parallel to the bit lines. Fig. 2 shows that the access transistors in adjacent columns are further apart than those in the same column. The fact that the enhancement is smaller by a factor of two is consistent with a greater separation of the sensitive drains along the bit-line direction than along the word-line direction.

Fig. 5 plots the total number of events (single-bits and double-bits) as a function of proton angle of incidence. There is

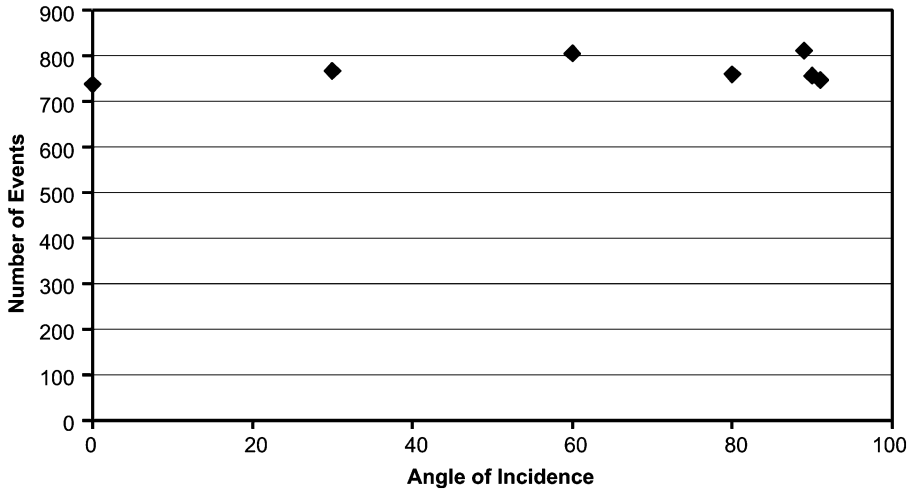

Fig. 7. Total number events (single-bit and double-bit) as a function of proton angle of incidence for 198 MeV protons incident on the NEC DRAM. The axis of rotation was parallel to the "bit" lines.

a reduction of about 25% going from normal incidence to 90°. We attribute this to a greater path length through the plastic package surrounding the part that the protons must traverse when incident near grazing angle. At normal incidence the protons travel through 0.42 mm of plastic before they reach the silicon, whereas for grazing incidence they can travel up to 5 mm through the plastic. Therefore, more protons are scattered away from the device at large angles of incidence, causing a reduction in the effective fluence and in the number of double-bit upsets. Furthermore, the average energy of the protons decreases with distance through the plastic and that causes a reduction in the cross section.

The same mechanisms previously invoked to explain the enhanced SEU cross section in the SOI device can also explain the effects observed for the DRAM–no increase in the number of single-bit errors with angle but a pronounced increase in the number of double-bit upsets. The absence of an increase in the number of single-bit upsets for both 63-MeV and 198-MeV protons at nonnormal incidence is due to the fact that the access transistor is formed in bulk silicon, where both drift and diffusion of charge contribute to the upset. Single-bit upsets are produced at normal incidence for both proton energies because of the large collection volume and low LET threshold. Since they already contribute at normal incidence, there cannot be any enhancement at large angles of incidence.

The situation is slightly different for double-bit upsets for which the requirement is that an ion track pass through or close to two sensitive volumes, separated laterally by a distance less than the range of the most energetic spallation ions. At normal incidence, a small number of laterally emitted spallation ions will be able to pass through both sensitive volumes and produce double-bit upsets. Most of the high-LET and long-range particles are forward scattered and do not contribute to double-bit upsets at normal incidence. At large angles of incidence, the forward-scattered particles, which are greater in number, will be able to traverse both junctions, and the number of double-bit upsets will increase.

The same argument may be used to explain the increase in the number of double-bit upsets with angle for 198-MeV protons. The only difference is that, at higher proton energies, all the particles emitted as a result of inelastic scattering have more energy. Therefore, at normal incidence many of those laterally emitted particles have sufficient range and energy to produce double bit upsets, so the enhancement is smaller. Fig. 6 shows that at normal incidence the number of double-bit upsets is greater but the maximum enhancement near grazing angle of incidence is smaller. The fact that the total number of events, shown in Fig. 7, does not decrease with angle of incidence for 198 MeV protons may be attributed to the much higher energy of the protons.

From the above discussion, three conclusions may be drawn regarding how the distance between the two closest access transistors affects the number of double-bit upsets. First, the number of double-bit upsets for normally incident protons will decrease as the distance increases. Second, the angle at which the number of double-bit upsets begins to exhibit an enhancement will increase with increasing distance. Third, the magnitude of the enhancement will decrease.

The discussion so far has not included charge collection via diffusion, which, for DRAMS in bulk silicon, is significant. The effect of diffusion is to increase the size of the charge-collection volumes for the two access transistors. That effectively reduces the distance between the closest access transistors, and causes a reduction in the angle at which enhancement begins, an increase in the number of double-bit upsets near normal incidence, and a smaller enhancement.

VII. Modeling

An attempt was made to qualitatively model the general trends of the experimental observations for proton-induced double-bit upsets using a modified version of the Clemson University Proton Interaction in Devices (CUPID) program [8]. Two volumes representative of the drains of the two closest access transistors were defined. Each volume was 0.2 μm thick and had lateral dimensions of 0.3 μm and 0.4 μm. The two volumes were separated by 0.6 μm. Inelastic scattering events were distributed randomly throughout the area encompassing

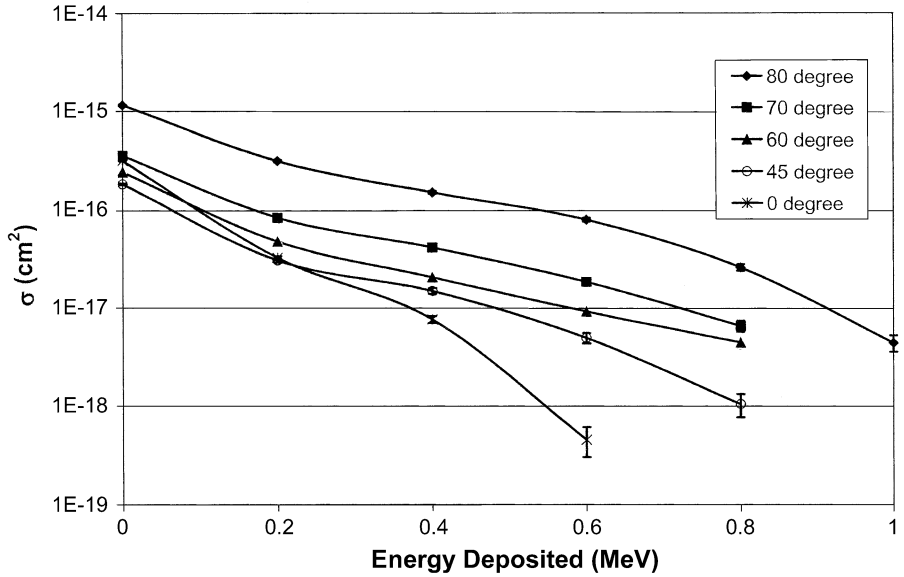

Fig. 8. Cross section for double-bit upsets as a function of deposited energy for 63 MeV protons calculated using CUPID. Each curve represents the results for a different angle of incidence.

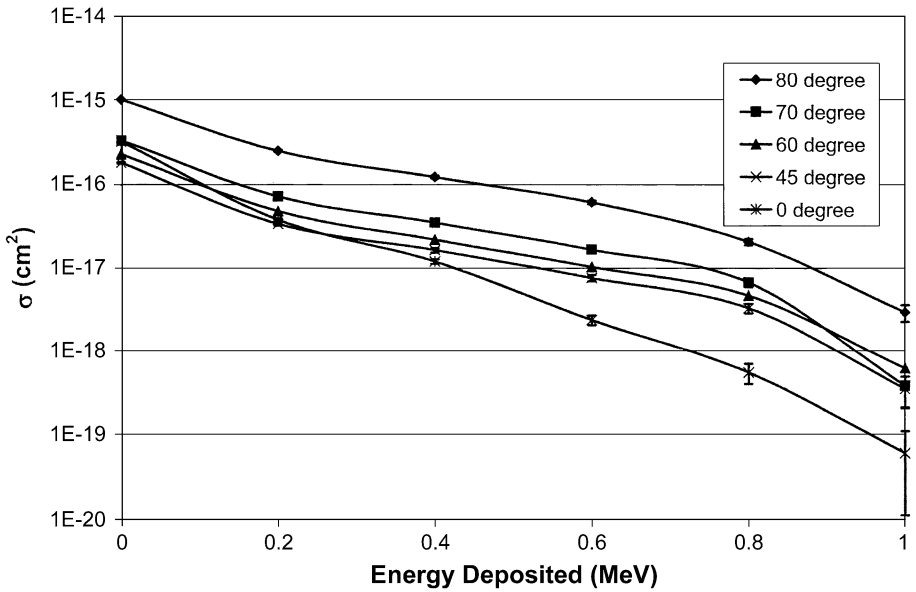

Fig. 9. Cross section for double-bit upsets as a function of deposited energy for 198 MeV protons calculated using CUPID. Each curve represents the results for a different angle of incidence.

the two sensitive volumes. The program tracked all emitted particles that traversed both volumes; it computed the cross section for depositing a certain amount of energy or greater in both volumes. Fig. 8 shows the results for 63 MeV protons and Fig. 9 for 198 MeV protons.

The results for the 63-MeV protons show that the cross section for double-bit upsets increases with increasing angle for all values of $Q_{\rm crit}$. For example, if the DRAM has a small $Q_{\rm crit}$ such that at least 0.2 MeV must be deposited in each of the two volumes to produce a double-bit upset, the cross section increases by approximately an order of magnitude between 0° and 80 °. However, if the DRAM has a larger $Q_{\rm crit}$ such that 0.5 MeV must be deposited in each volume to produce a double-bit upset, the overall cross sections are reduced, but the enhancement with angle is seen to increase by more than two orders of magnitude between 0° and 80°.

The results for 198 MeV protons show similar trends, only less pronounced. The cross section increases with increasing angle of incidence, and the increase is greater for devices with a larger $Q_{\rm crit}$.

The results displayed in Figs. 8 and 9 are not quantitatively accurate because the model does not include charge collection by diffusion. Diffusion is known to play a significant role in DRAMs manufactured in bulk silicon, so this shortcoming points to a major limitation of the CUPID code as currently implemented. However, the overall trends observed experimentally are in qualitative agreement with the results of modeling with CUPID.

VIII. Conclusion

The cross section for double-bit upsets in a 16-Mbit DRAM irradiated with protons increases with increasing angle of incidence. On the other hand, the cross section for single-bit upsets does not. The enhancement was found to depend on proton energy and on critical charge. Modeling results using CUPID agree with the overall trends but, because they do not include diffusion, only qualitative trends can be studied.

Multiple-bit upsets are of concern because one commonly used error detection and correction method, Hamming Code, is able to detect and correct only one error in a word. Two or more errors in a word can be detected but not corrected.

The results presented here are for a relatively old technology with large distances ($\sim 1\ \mu$m) between devices. Modern bulk DRAM technologies with more closely spaced memory cells ($0.1\ \mu$m) should show a greater sensitivity for multiple-bit upsets. How those multiple-bit upsets depend on proton angle of incidence will be an interesting area of investigation.

Acknowledgment

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